Analog vs. digital interleaving of PFC converters

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Power supplies in large systems that have input power of over 1kW typically use power factor correction (PFC) for various reasons. Recent advances in PFC include interleaving of two out-of-phase circuits to gain many system level advantages. Enough has been discussed about the advantages of interleaved PFC; this article focuses on a comparison of the analog approach to the digital approach.

The interleaving of PFC converters using analog controllers requires very sophisticated ICs that are dedicated for this purpose because of multiple loops within the system. A system based on analog controllers is forced to achieve a balance between complexity of the system and flexibility for adoption to various application needs. On the other hand, using an MCU to manage the feedback loop and management of peripheral functions provides utmost flexibility with only a slight increase in complexity.

Digital approach has two different meanings. One is the management of peripheral functions, which is commonly referred to as "digital management," and the other is feedback loop control, which is called "digital control." Digital control, compared to analog control (of a feedback loop), does not really offer huge advantages; it is the combination of a digital control loop with digital management that creates a value that is more than a complete analog system.

MCU-based converters can measure and report the input power. The same input power measurement data can also be used internally to alter and optimize output voltage and switching frequency. Hence, with MCU-based converters, efficiency is optimized to the highest level and the efficiency curve can be flattened. Also, when demand for power is less than a certain threshold, one or more phases can be shut down to improve low load efficiency.

The cost of power components such as magnetics, MOSFETs and diodes, in higher power SMPS is significantly higher compared with the cost of controllers. Hence, any saving in power components is easily paid off even if it requires higher cost in control components. Design for short circuit, power-up and power-down sequencing sometimes stresses power components beyond their normal operating level leading to the over-design of such components. With the help of the fuzzy logic of MCUs, it is very easy to implement timing and controls to minimize this over-design and reduce the overall cost of the system.

A test board based on ST's STM32F103 was designed to run at the 100W power level, 100kHz switching frequency, with universal input range, and an output voltage of 400V. Because the timers of the STM32 can be triggered from one to the next with a precise time offset, it is possible to do interleaving, with as many phases as needed, limited by the number of timers on the device. Our testing showed good efficiency even with the overhead of startup power regulators needed to boot up the MCU first.

An MCU-based system also allows management of other functions in the SMPS that are beyond the realm of PFC, such as inrush current control and communication with the external world. A simple and cost-effective inrush current control can be implemented by using a resistor to limit the inrush current at start-up and then jumping the resistor out by means of a relay. A thermistor in contact

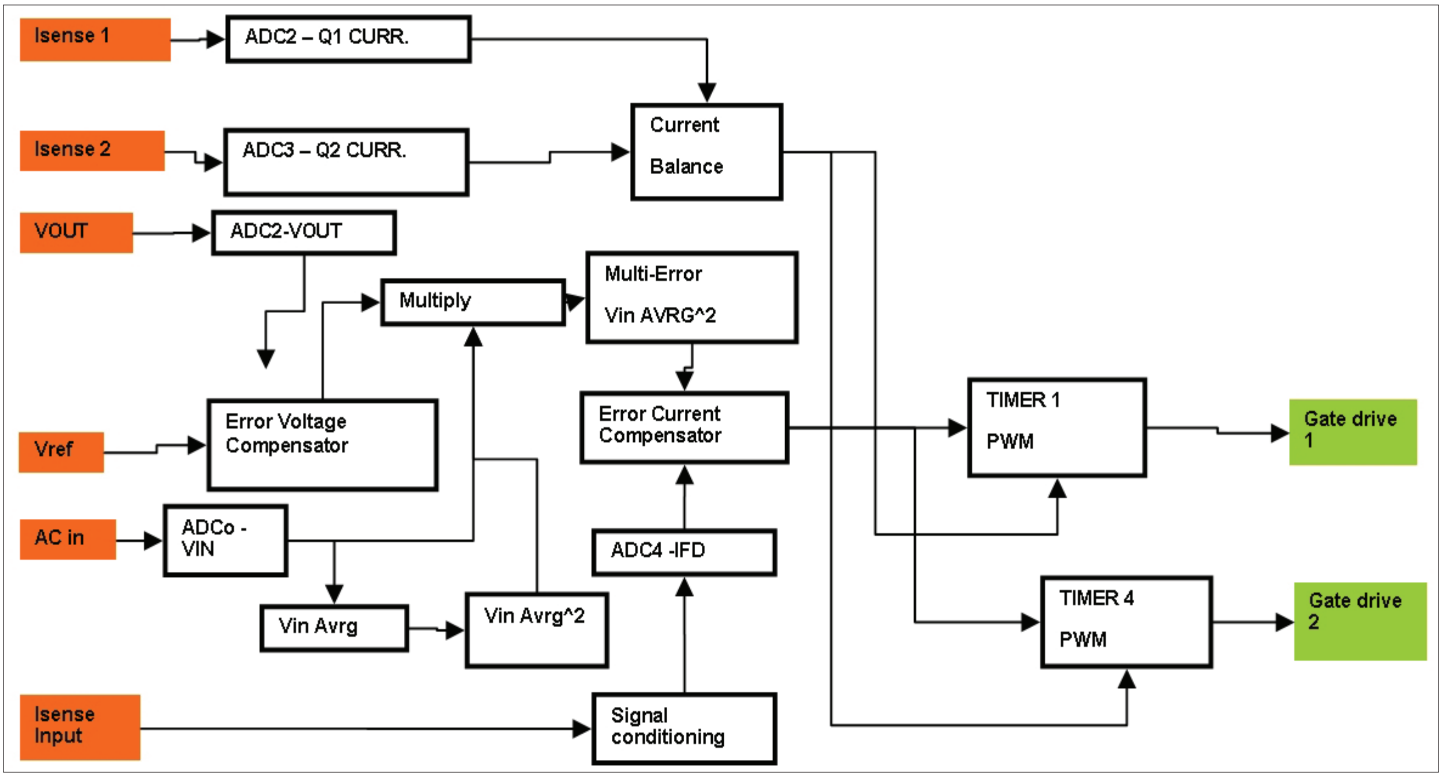

Figure 1: Shown is the functional block diagram of a typical interleaved PFC circuit with 2 phases based on ST's STM32F103 MCU.

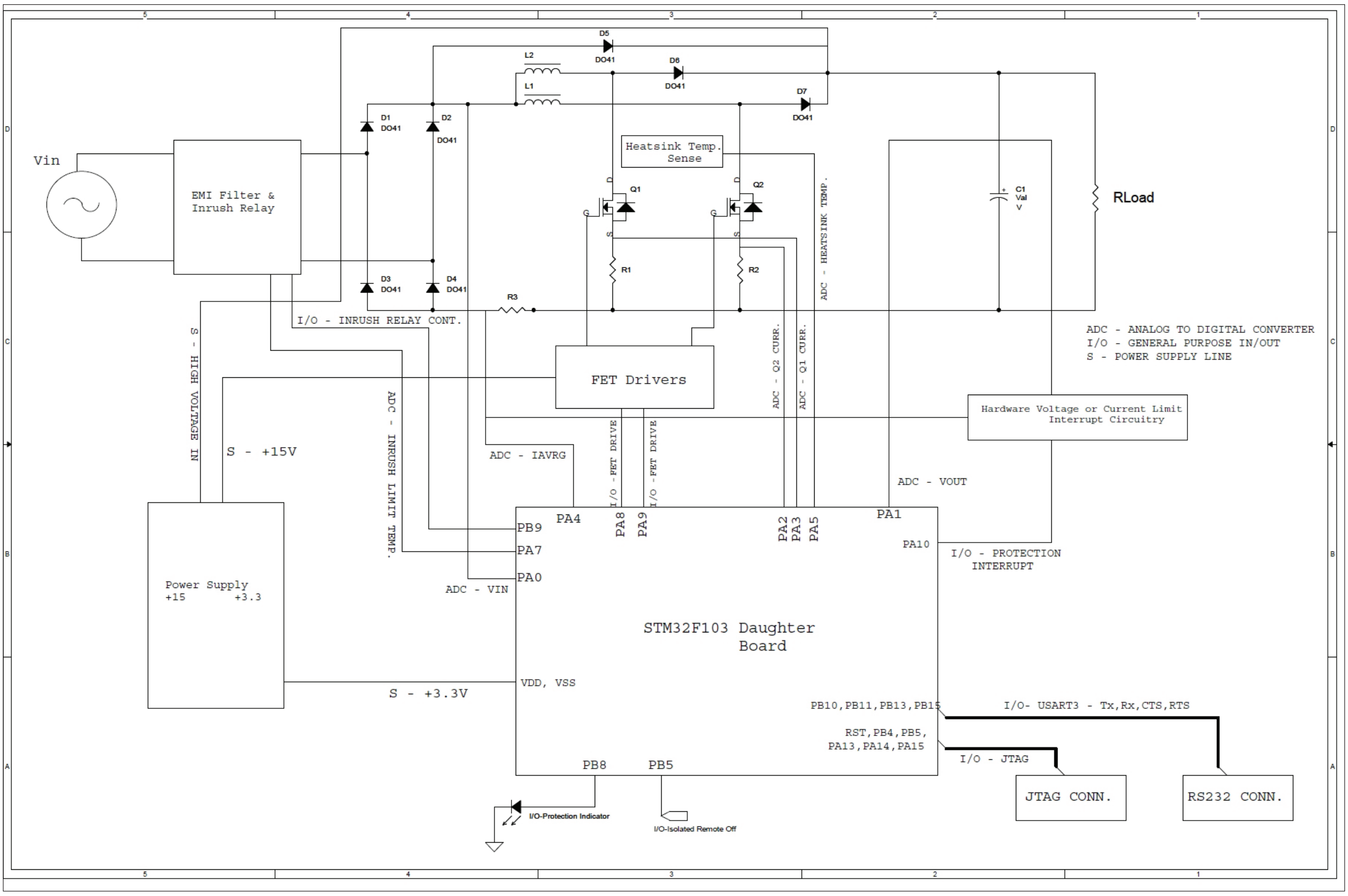

Figure 2: Shown is the component level block diagram.

with the resistor can be used to detect relay failures and prevent false startups of the circuit.

One or more thermistors in contact with major power components can be used to sense internal temperatures of the system, which can then be reported to the external world. Moreover, the same information can be used to implement a precise fan speed control system by using a simple lookup table. With digital control, it is very easy to set boundary conditions to set operating limits for the converter and reduce waste of over designing in the system for taking care of abnormal operating conditions. An MCU-based system also reduces variations in the control module from one platform to another platform, compared with their analog counterparts, reducing engineering development time of future projects.

A functional block diagram of a typical interleaved PFC circuit with 2 phases based on ST's STM32F103 MCU is shown in **Figure 1**.

Output of the system is a gate drive signal for the MOSFETs of the two phases of the interleaved converter. Inputs to the system, from the external world, are Voltage reference (Vref), Output voltage (Vout) and AC input voltage (AC in). Internally generated inputs to the digital control loop are Input AC current (Isense input), Instantaneous current of phase 1 (Isense 1) and Instantaneous current of phase 2 (Isense 2).

The block diagram shows the three critical inputs used in the control blocks of the PFC circuit. These three inputs include voltage on ADC0, the boost output voltage on ADC2 and the current feedback signal on ADC4. The measured input voltage is used in two control functions: The first one is used as one of the inputs of the multiply calculation that along with the error term is used to shape the current waveform. The second one is used to determine the average input voltage used in figuring the maximum allowable current so that the maximum allowable power can be kept constant as the input voltage range changes. The output voltage is sensed by an ADC and compared to a numerical constant in the code. Based on that, an error term is calculated and multiplied with the instantaneous input voltage to shape the current waveform to match the input voltage wave form. By further dividing this by the square of the average input voltage, a current reference (Iref in the diagram) is established and is used to program the current compensator. The current compensator uses the last critical input, which is the current feedback level converted on ADC4. Implemented as a PID loop, the current compensator uses the Iref level as the set point and the ADC4 level as the process variable. The output of the loop programs the duty cycle of the MOSFET switches via peripheral timers one and four.

The inputs ADC2 and ADC3 measure the currents flowing in the boost MOSFETs of the two phases. With both converters being fed from the same voltage source, having equal value inductors and driven with the same value duty cycles, the average currents in the two phases share the output current almost equally. The measured values are compared relative to each other and if there is a large difference between the two currents, indicating trouble, the outputs are shut down and an error is reported via the communications link.